

PRODUCT SPECIFICATION FOR OLED MODULE

Revision: V1.0

Model No: 0.96-4PIN(NEW) CIR

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1. FUNCTIONS & FEATURES

• LCD TYPE:

MODULE MODEL	LCD TYPE	REMARK
2864KLWEG01	0.96" OLED Passive Matrix	

Driving Scheme : 1/64 Duty,
Viewing direction : 6 O'clock
Drive IC : SSD1315

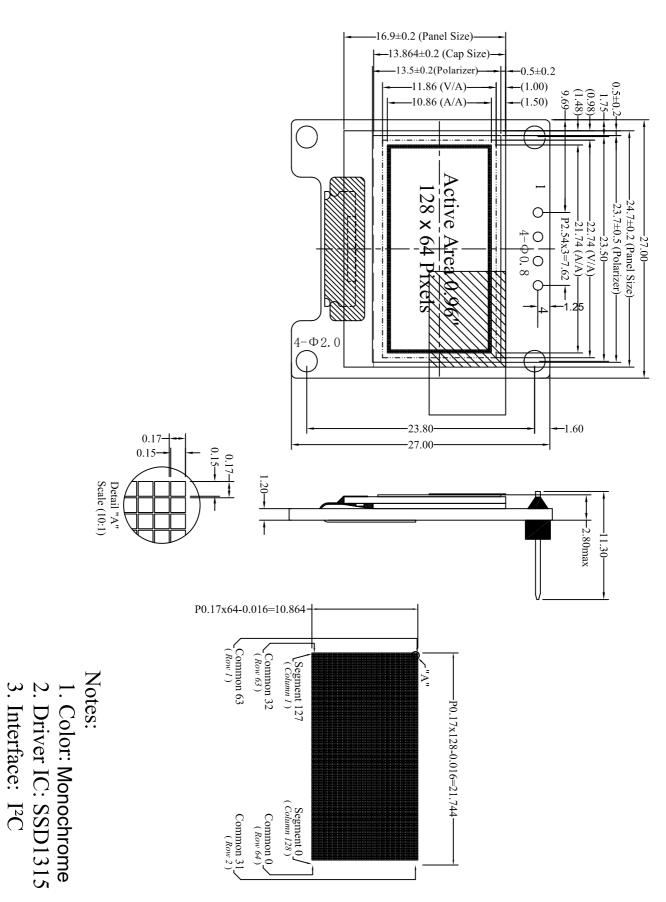
 $\begin{array}{ll} \bullet & \text{Power Supply Voltage} & : 3.0 \text{V} \\ \bullet & \text{V}_{\text{CC}} & : 12.0 \text{V} \\ \bullet & \text{Interface} & : \text{IIC} \end{array}$

RoHS Compliant

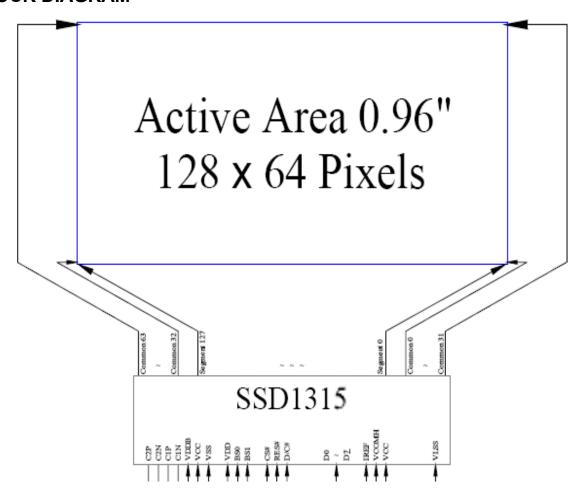
2. MECHANICAL SPECIFICATIONS

Module Size
 Viewing Area
 Active Area
 Dot Pitch
 Dot Size
 27(L)X27(W)X11.3Max(T)mm
 22.74(L) x 11.86 (W) mm
 21.74 (L) x 10.86 (W) mm
 0.154 (W) x 0.154 (H) mm
 0.17(W) x 0.17(H) mm

3. EXTERNAL DIMENSIONS (♥☐ unit: mm)



4. BLOCK DIAGRAM



5. PIN ASSIGNMENT

PIN	SYMBOL	Descriptions							
1	GND	Ground of Logic Circuit							
2	VDD	Power Supply for Logic							
3	SCK	Serial clock input.							
4	SDA	Serial data input.							

6. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V _{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V _{cc}	0	16	V	1, 2
Supply Voltage for DC/DC	V _{BAT}	-0.3	5	V	1, 2
Operating Temperature	T _{OP}	-40	85	°C	
Storage Temperature	T _{STG}	-40	85	°C	3
Life Time (120 cd/m²)		10,000	-	hour	4
Life Time (80 cd/m²)		30,000	-	hour	4
Life Time (60 cd/m²)		50,000	-	hour	4

Note 1: All the above voltages are on the basis of " $V_{SS} = 0V$ ".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 12.0V, T_a = 25°C, 50% Checkerboard.

Software configuration follows Section 4.4 Initialization.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

7. ELECTRICAL CHARACTERISTICS

7.1. Optics Characteristics

Characteristics	Symbol	Conditions	Min	Тур	Max	Unit
Brightness (V _{cc} Supplied Externally)	L_{br}	Note 5	80	100	-	cd/m²
Brightness (V _{CC} Generated by Internal DC/DC)	L _{br}	Note 6	50	60	-	cd/m²
C.I.E. (Blue)	(x) (y)	C.I.E. 1931	0.10 0.20	0.14 0.24	0.18 0.28	
C.I.E. (Yellow)	(x) (y)	C.I.E. 1931	0.43 0.45	0.47 0.49	0.51 0.53	
Dark Room Contrast	CR		-	2000:1	-	
Viewing Angle			-	Free	-	degree

^{*} Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12V & 7.25V. Software configuration follows Section 4.4 Initialization.

7.2. DC CHARACTERISTICS

Characteristics	Symbol	Conditions	Min	Тур	Max	Unit
Supply Voltage for Logic	V _{DD}		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	Vcc	Note 5 (Internal DC/DC Disable)	11.5	12.0	12.5	v
Supply Voltage for DC/DC	V_{zar}	Internal DC/DC Enable	3.5	-	4.2	ν
Supply Voltage for Display (Generated by Internal DC/DC)	Vcc	Note 6 (Internal DC/DC Enable)	7.0	-	7.5	ν
High Level Input	V_{IH}	I _{OUT} = 100μA, 3.3MHz	0.8×V _{DD}	-	V_{DD}	v
Low Level Input	V_{IL}	I _{OUT} = 100μA, 3.3MHz	0	-	0.2×V _{DD}	v
High Level Output	V _{OH}	I _{OUT} = 100μA, 3.3MHz	0.9×V _{DD}	-	V _{DD}	v
Low Level Output	V _{OL}	I _{OUT} = 100μA, 3.3MHz	0	-	0.1×V _{DD}	v
Operating Current for V _{DD}	I _{DD}		-	180	300	μΑ
Operating Current for V _∞ (V _∞ Supplied Externally)	I _{CC}	Note 7	-	12.3	16	mA
Operating Current for V_{MI} (V_{CC} Generated by Internal DC/DC)	$I_{ extit{DAT}}$	Note 8	-	21	28.0	mΑ
Sleep Mode Current for V _{DD}	I _{DD, SLEEP}		-	1	5	μΑ
Sleep Mode Current for V _{CC}	I _{CC, SLEEP}		-	2	10	μΑ

Note 5 & 6: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 7: $V_{DD} = 2.8V$, $V_{CC} = 12V$, 100% Display Area Turn on. Note 8: $V_{DD} = 2.8V$, $V_{CC} = 7.25V$, 100% Display Area Turn on.

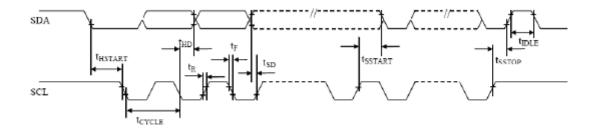
^{*} Software configuration follows Section 4.4 Initialization.

7.3.AC CHARACTERISTICS

1 I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t _{cycle}	Clock Cycle Time	2.5	-	μs
t _{HSTART}	Start Condition Hold Time	0.6	-	μs
	Data Hold Time (for "SDA _{OUT} " Pin)	0		
t _{HD}	Data Hold Time (for "SDA _{IN} " Pin)	300	_	ns
t _{SD}	Data Setup Time	100	-	ns
t _{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t _{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t _R	Rise Time for Data and Clock Pin		300	ns
t _F	Fall Time for Data and Clock Pin		300	ns
t _{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs

^{* (}V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



8. COMMANDS

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

1. Fu	ındame	ntal (omm	and T	able						
D/C#	#Hex	D 7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	81	1	0	0	0	0	0	0	1	Set Contrast Control	Double byte command to select 1 out of 256
0	A[7:0]	A_7	A_6	A_5	A_4	A ₃	A_2	Aı	A_0		contrast steps. Contrast increases as the value
											increases.
											(RESET = 7Fh)
$oxed{oxed}$											
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X ₀ =0b: Resume to RAM content display
											(RESET)
											Output follows RAM content A5h, X ₀ =1b: Entire display ON
											Output ignores RAM content
h	A6/A7	1	0	1	0	0	1	1	Χo	Set Normal/Inverse	A6h, X[0]=0b: Normal display (RESET)
٢	AU/A/	1	ľ	1	"	١ ٠	1	*	Δ0	Display	0 in RAM: OFF in display panel
										Display	1 in RAM: ON in display panel
											A7h, X[0]=1b: Inverse display
											0 in RAM: ON in display panel
											1 in RAM: OFF in display panel
0	ΑE	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode)
	AF										(RESET)
											AFh X[0]=1b:Display ON in normal mode
I	1	I	I	I	I	I	I	1	I	1	

2. S	crolling (Com	mand	l Tab	le						
D/C	#Hex	D 7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26/27	0	0	1	0	0	1	1	X_0	Continuous	26h, X[0]=0, Right Horizontal Scroll
0	A[7:0]	0	0	0	0	0	0	0	0	Horizontal Scroll	
0	B[2:0]	*	*	*	*	*	B_2	B_1	B ₀	Setup	(Horizontal scroll by 1 column)
0	C[2:0]		*	*	*	*	C ₂	C ₁	C ₀		A[7:0]: Dummy byte (Set as 00h)
0	D[2:0]		*	*	*	*	D_2	D_1	D ₀		B[2:0] : Define start page address
0	E[7:0]		0	0	0	0	0	0	0		000b - PAGE0 011b - PAGE3 110b - PAGE6
0	F[7:0]		1	1	1	1	1	1	1		001b - PAGE1 100b - PAGE4 111b - PAGE7
ľ	[]	-	-	-	-	-	-	-	-		010b - PAGE2 101b - PAGE5
											C[2:0] : Set time interval between each scroll step in
											terms of frame frequency
											000b - 5 frames 100b - 3 frames
											001b - 64 frames 101b - 4 frames
											010b - 128 frames 110b - 25 frame
											011b - 256 frames 111b - 2 frame
											D[2:0] : Define end page address
											000b - PAGE0 011b - PAGE3 110b - PAGE6
											001b - PAGE1 100b - PAGE4 111b - PAGE7
											010b - PAGE2 101b - PAGE5
											The value of D[2:0] must be larger or equal
											to B[2:0]
											E[7:0] : Dummy byte (Set as 00h)
											F[7:0]: Dummy byte (Set as FFh)

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2. Scr	olling (Comi	nand	Tab	le						
D/C#		D7			D4	D3	D2	D1	D0	Command	Description
D/C# 0 0						D3 1 0 * * E ₃	00 00 B ₂ C ₂ D ₂ E ₂	D1 X ₁ 0 B ₁ C ₁ D ₁ E ₁	D0 X ₀ 0 B ₀ C ₀ D ₀ E ₀	Continuous Vertical and	Description
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Note 13 No continuous vertical scrolling is available. Stop scrolling that is configured by command 26h/27h/29h/2Ah.
											Note 1) After sending 2Eh command to deactivate the sceolling action, the ram data needs to be rewritten.
0	E C	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup commands :26h/27h/29h/2Ah with the following valid sequences: Valid command sequence 1: 26h; 2Fh. Valid command sequence 2: 27h; 2Fh. Valid command sequence 3: 29h; 2Fh. Valid command sequence 4: 2Ah; 2Fh. For example, if "26h; 2Ah; 2Fh." commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.

Sc	rolling (Com	mand	Tab	le						
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A3 A[5:0] B[6:0]	1 * *	0 * B ₆	1 A ₅ B ₅	0 A ₄ B ₆	0 A ₃ B ₃	0 A ₂ B ₂	1 A ₁ B ₁	1 A ₀ B ₀	Area	A[5:0]: Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0] B[6:0]: Set No. of rows in scroll area. This is the mumber of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64] Note A[5:0]+B[6:0] ← MUX ratio A[5:0]+B[6:0] ← MUX ratio A[6:0] ← MUX ratio Set Display Start Line (X ₅ X ₆ X ₃ X ₂ X ₁ X ₀ of 40b∼7Fh) ← B[6:0] The last row of the scroll area shifts to the first row of the scroll area. For 64d MUX display A[5:0] = 0, B[6:0]=64: whole area scrolls A[5:0] = 0, B[6:0] < 64: top area scrolls A[5:0] + B[6:0] < 64: central area scrolls A[5:0] + B[6:0] = 64: bottom area scrolls

Product Specification

3. A	ddressin	ng Set	ting (omm	and T	able					
D/C#								D1	D0	Command	Description
0	00~0F	0	0	0	0	X ₃	X ₂	X ₁	X ₀	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. Note 1) This command is only for page addressing mode
О	10∼1F	0	0	0	1	X ₃	X_2	X ₁	X ₀	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. Note This command is only for page addressing mode
-	20 A[1:0]	0 *	0 *	1 *	0 *	0	0	0 A ₁		Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0	21 A[6:0] B[6:0]	0 * *	0 A ₆ B ₆	1 A ₅ B ₅	0 A ₄ B ₄	0 A ₃ B ₃	0 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀	Set Column Address	Setup column start and end address A[6:0]: Column start address, range: 0-127d, (RESET=0d) B[6:0]: Column end address, range: 0-127d, (RESET =127d) Note This command is only for horizontal or vertical addressing mode.

	3. Addressing Setting Command Table										
D/C	#Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	22	0	0	1	0	0	0	1	0	Set Page Address	Setup page start and end address
0	A[2:0]	*			*		A_2	A_1	A_0		A[2:0] : Page start Address, range : 0-7d,
0	B[2:0]	*			*		B_2	B ₁	B ₀		(RESET = 0d)
l											B[2:0] : Page end Address, range : 0-7d,
l						1					(RESET = 7d)
l				l		1	1	1	1		Note
l						1					⁽¹⁾ This command is only for horizontal or vertical addressing mode.
											suchessing mode.
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start	Set GDDRAM Page Start Address
l						1	1	l .	"	Address for Page	(PAGE0~PAGE7) for Page Addressing Mode
l						1				Addressing Mode	using X[2:0].
l						1					
l						1	1				Note
											¹⁾ This command is only for page addressing mode

Product Specification

4. Ha	4. Hardware Configuration (Panel resolution & layout related) Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	
b	40~7F	0	1	X,	X4	X_3	X ₂	Xı	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using X ₂ X ₃ X ₂ X ₃ X ₀ . Display start line register is reset to 000000b during RESET.	
b	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0	
0	A8 A[5:0]	1 *	0 *	1 A ₅	0 A ₄	1 A ₃	0 A ₂	0 A ₁	0 A ₀	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.	
D	C0/C8	1	1	0	0	X ₃	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N-1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.	
0	D3 A[5:0]	1	1	0 A ₅	1 A4	0 A ₃	0 A ₂	1 A ₁	1 A ₀	Set Display Offset	Set vertical shift by COM from 0d-63d The value is reset to 00h after RESET.	
0	DA A[5:4]	1 0	0	0 A ₅	1 A ₄	0	0	1	0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b(RESET), Alternative COM pin configuration A[5]=0b(RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap	

 Tit 	5. Timing & Driving Scheme Setting Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description	
1-	D5 A[7:0]	l A,	1 A ₆	0 A ₅	1 A ₄	0 A ₃	1 A ₂	0 A ₁	1 A ₀	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0]: Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4]: Set the Oscillator Frequency, Fosc. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b Range:0000b~1111b Frequency increases as setting value	
	D9 A[7:0]	1 A ₇	1 A ₆	O As	1 A4	1 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Pre-charge Period	increases. A[3:0]: Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h) A[7:4]: Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)	
Γ.	DB A[6:4]	0	1 A ₆	0 A ₅	1 A ₄	0	0	1 0	1 0	Set V _{COMH} Deselect Level	A[6:4] Hex V COMH deselect level	
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation	

Note
(1) "a" stands for "Don't care".

9. FUNCTIONAL SPECIFICATION

.1 Commands

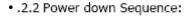
Refer to the Technical Manual for the SSD1306

.2 Power down and Power up Sequence

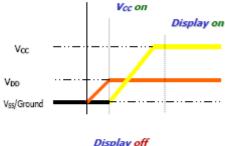
To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

.2.1 Power up Sequence:

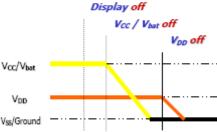
- 1. Power up V_{DD}
- 2. Send Display off command
- 3. Initialization
- 4. Clear Screen
- 5. Power up V_{CC}/ V_{BAT}
- Delay 100ms (When V_{CC} is stable)
- 7. Send Display on command



- 1. Send Display off command
- Power down V_{CC} / V_{BAT}
- Delay 100ms (When V_{CC} / V_{BAT} is reach 0 and panel is completely discharges)
- 4. Power down VDD



VDD / VBAT OR



Note 13:

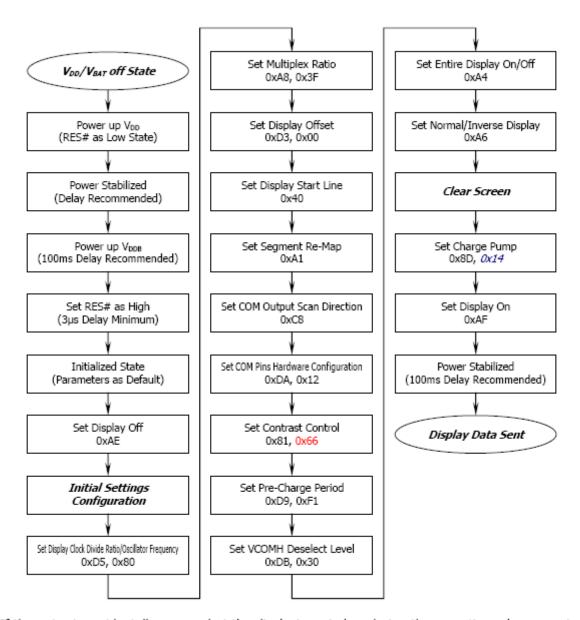
- Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
- V_{CC} / V_{BAT} should be kept float (disable) when it is OFF.
- Power Pins (V_{DD}, V_{CC}, V_{BAT}) can never be pulled to ground under any circumstance.
- 4) VDD should not be power down before VCC / VBAT power down.

.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

- 1. Display is OFF
- 2. 128×64 Display Mode
- Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
- 4. Shift register data clear in serial interface
- 5. Display start line is set at display RAM address 0
- 6. Column address counter is set at 0
- 7. Normal scan direction of the COM outputs
- 8. Contrast control register is set at 7Fh
- 9. Normal display mode (Equivalent to A4h command)

.4 Actual Application Example



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence> Power Stabilized Normal Operation VDD/VBAT off State (100ms Delay Recommended) Power down V_{BAT} Set Display Off 0xAE (50ms Delay Recommended) Set Charge Pump Power down V_{DD} 0x8D, 0x10 <Entering Sleep Mode> Set Charge Pump Normal Operation Sleep Mode 0x8D, 0x10 Set Display Off Power down V_{BAT} 0xAE <Exiting Sleep Mode> Set Charge Pump Power Stabilized Sleep Mode 0x8D, 0x14 (100ms Delay Recommended) Power up V_{BAT} Set Display On Normal Operation (100ms Delay Recommended) 0xAF

10. MODULE ACCEPT QUALITY LEVEL (AQL)

10.1 AQL Standard Value: Critical Defect =0.1, Major Defect=0.65; Minor Defect =2.5.
10.2 Inspection Standard: MIL-STD-105E Table Normal Inspection Single Sampling Level II

11. RELIABILITY TEST.

· · .1 Contents of Reliability Tests

Item	Conditions	Criteria	
High Temperature Operation	70°C, 240 hrs		
Low Temperature Operation	-40°C, 240 hrs	The operational functions work.	
High Temperature Storage	85°C, 240 hrs		
Low Temperature Storage	-40°C, 240 hrs		
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs		
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell		

^{*} The samples used for the above tests do not include polarizer.

· · .2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at $23\pm5^{\circ}$ C; $55\pm15^{\circ}$ RH.

12. QUALITY DESCRIPTION & APPLICTION NOTE

Please refer to "General Inspection Criteria" document.

^{*} No moisture condensation is observed during tests.